

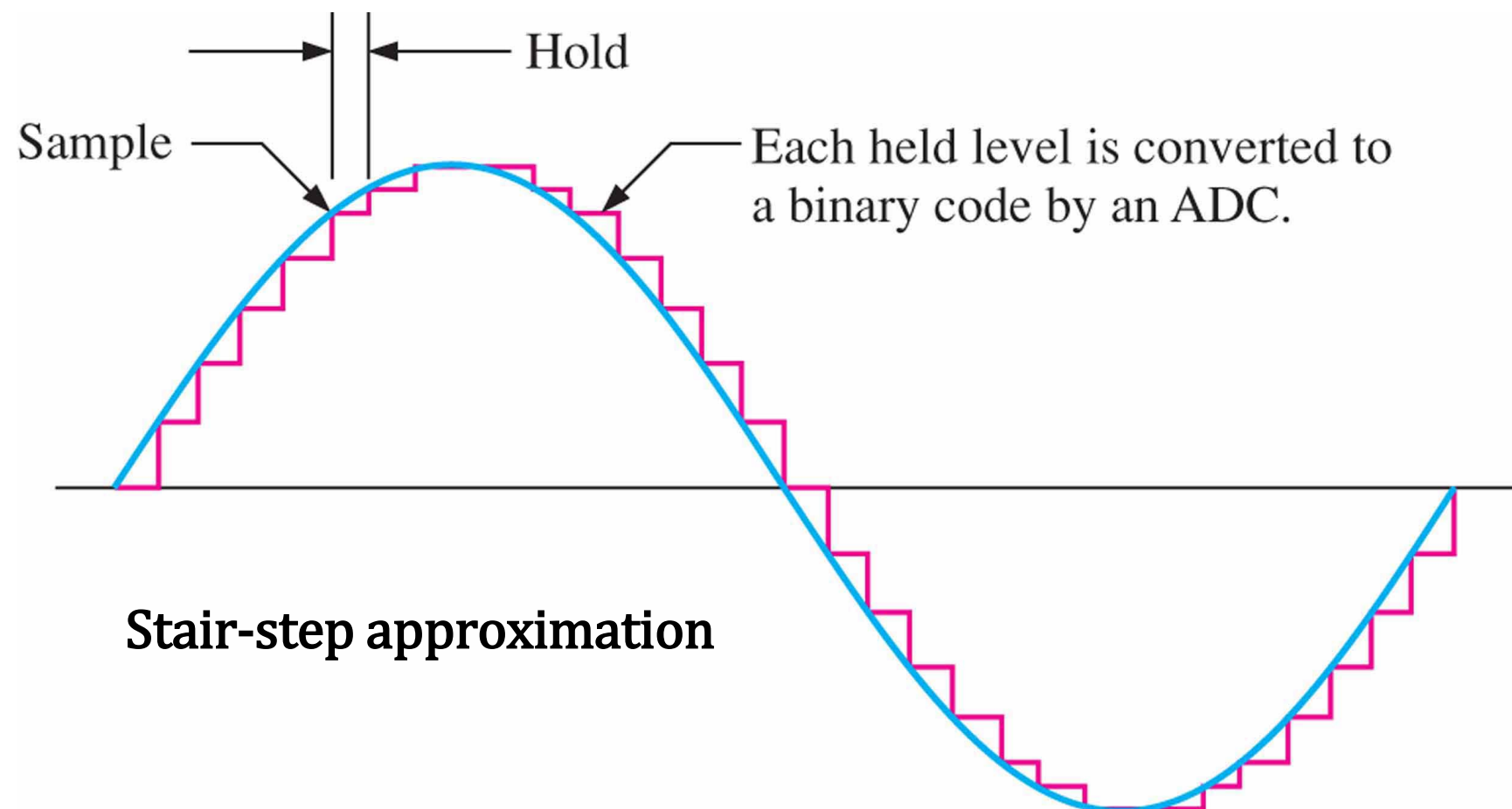
EES 271 Digital Circuits

Lecture 14 ~ D/A and A/D Conversions

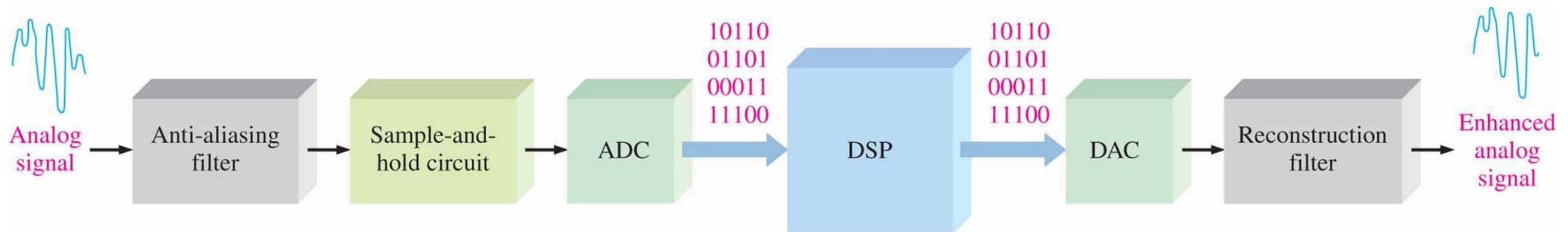
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Data Acquisition

- A **data acquisition** (DAQ) unit converts signals that naturally occur in analog form, such as sound, video, and information from sensors, to digital form that can easily be stored, modified and transmitted.
- The first step involves the translation of a continuously varying analog signal into a series of discrete levels resembling a staircase. This process (**stair-step approximation**) is accomplished by a **sample-and-hold circuit**.



- Next, the stair-step approximation is **quantized** into binary codes that represent each discrete step by a process called **analog-to-digital conversion**. The circuit that performs A/D conversion is called an **analog-to-digital converter** (ADC).
- Once the analog signal has been converted to a binary coded form, it is applied to a digital signal processor which can perform various operations on the incoming data:
 - ✦ Removing unwanted interference.
 - ✦ Increasing the amplitude of some signal frequencies, while reducing others.
 - ✦ Encoding the data for secure transmission.
 - ✦ Detecting and correcting errors in transmitted codes.
- After a DSP processes a signal, it can be converted back to a much improved version of the original analog signal using a **digital-to-analog converter** (DAC).



Example of basic data acquisition (DAQ) system

Sampling and filtering

- The first two processes of a DSP system are the **anti-aliasing filter** and the **sample-and-hold circuit**.
- **Sampling** refers to the process of taking a sufficient number of discrete values at points on a waveform that will define the shape of that waveform. The more samples you take, the more accuracy you will have.
- This will convert an analog signal into a series of impulses, each representing the amplitude of the signal at a given instant in time.

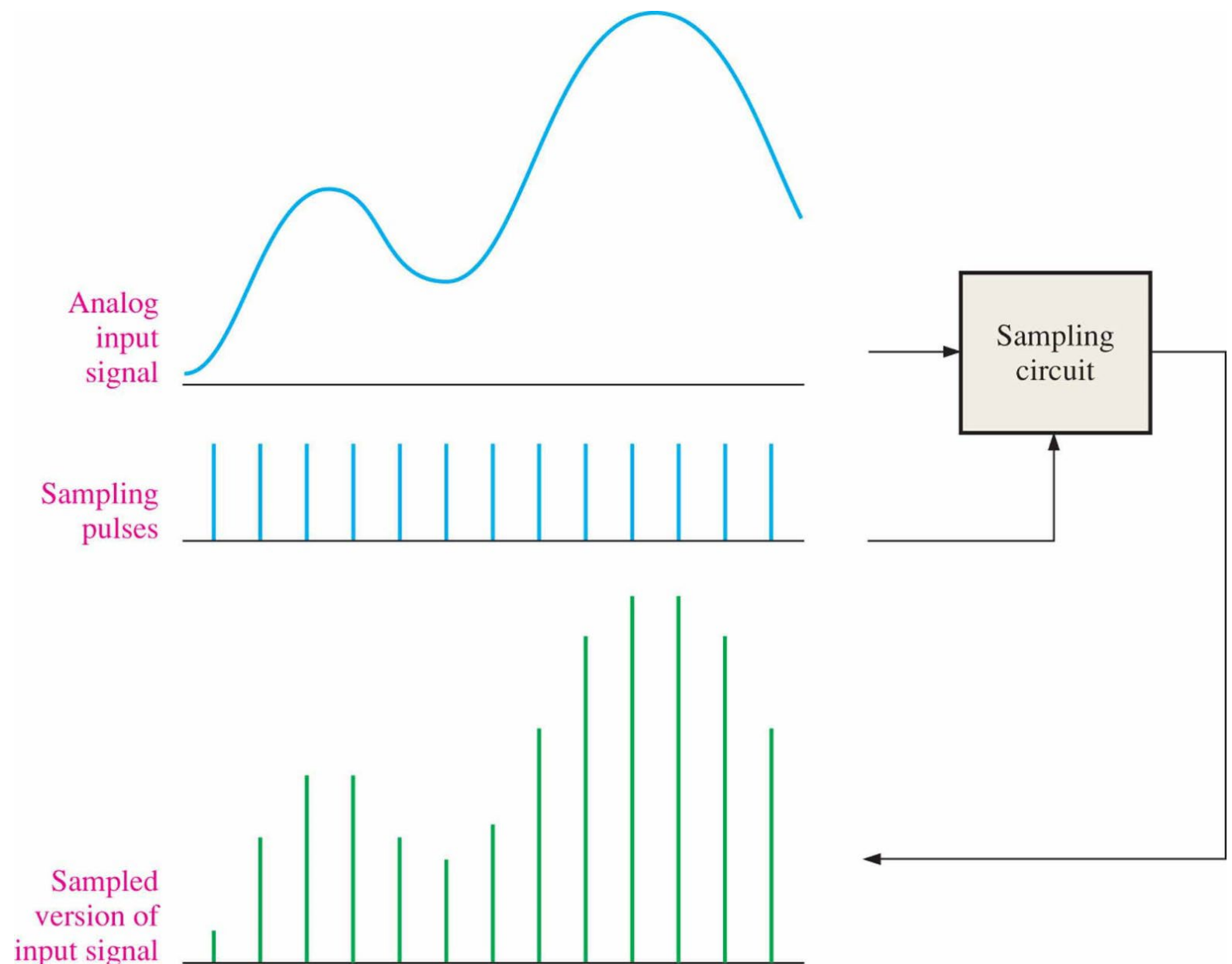
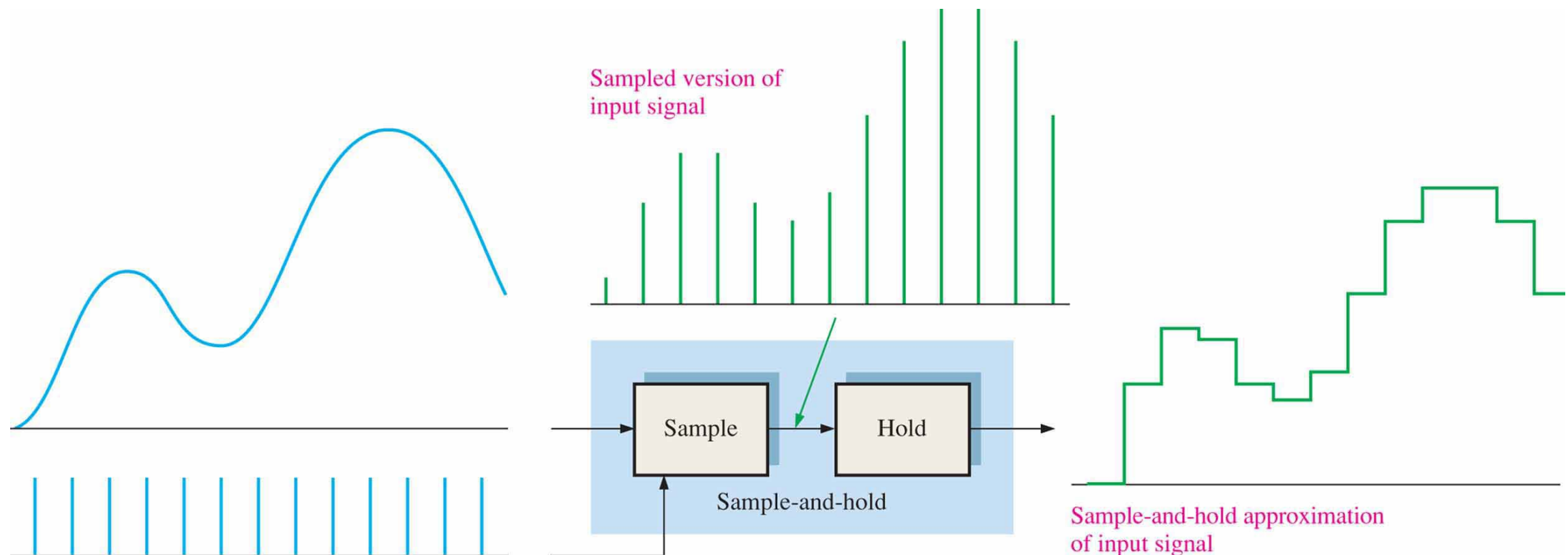


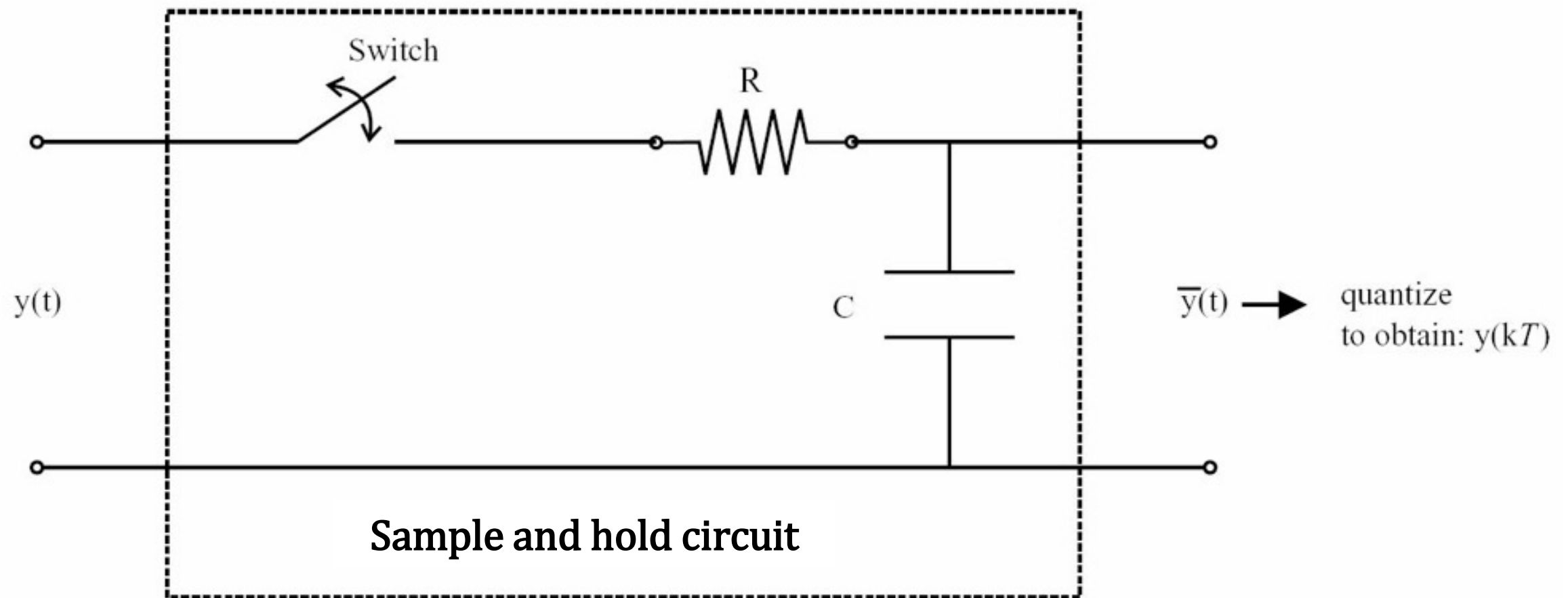
Illustration of the sampling process

Holding the Sampled Value

- The holding operation is part of the **sample-and-hold block**.
- After filtering and sampling, the sampled level must be held constant until the next sample occurs.
- This is necessary for the ADC to have time to process the sampled value. This sample-and-hold operation results in a **stair-step waveform** that approximates the analog input waveform.



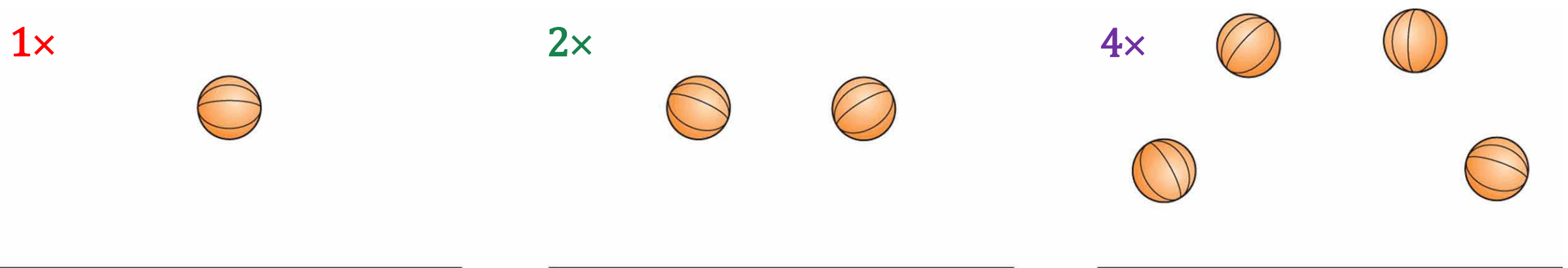
Sampling Circuit



- A typical **sample and hold circuit** shown above.
 - ✦ When the switch is turned ON, the output will track the input signal (**sampling operation**).
 - ✦ When the switch is turned OFF, the output will stay constant at the last value (**hold operation**).

The Sampling Theorem

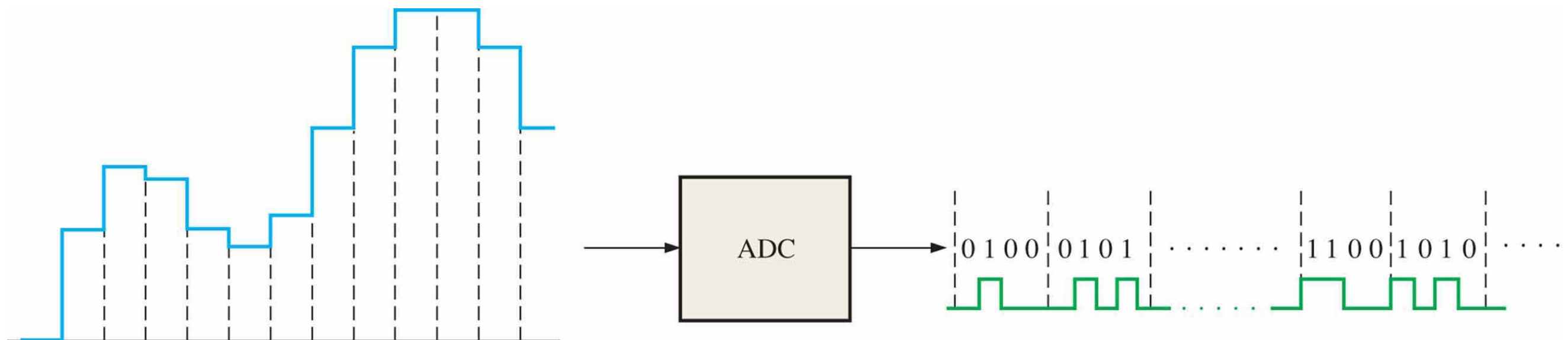
- All analog signals (except a pure sine wave) contain a spectrum of frequencies call **harmonics** (sine waves of different frequencies and amplitudes). When the harmonics or a given periodic waveform are added, the result is the original signal.
- Before a signal can be sampled, it must be passed through a **low-pass or anti-aliasing filter** to remove harmonic frequencies above a certain value as determined by the **Nyquist frequency**.
- The sampling theorem states that the **sampling frequency** must be at least twice the highest frequency component of the analog signal. This only preserves the frequency of the signal. In practice, to keep the shape of the waveform, the sampling frequency should be at least 10 times as fast as the signal.



Snapshots of a bouncing basketball at different sampling frequencies

Analog-to-Digital Conversion

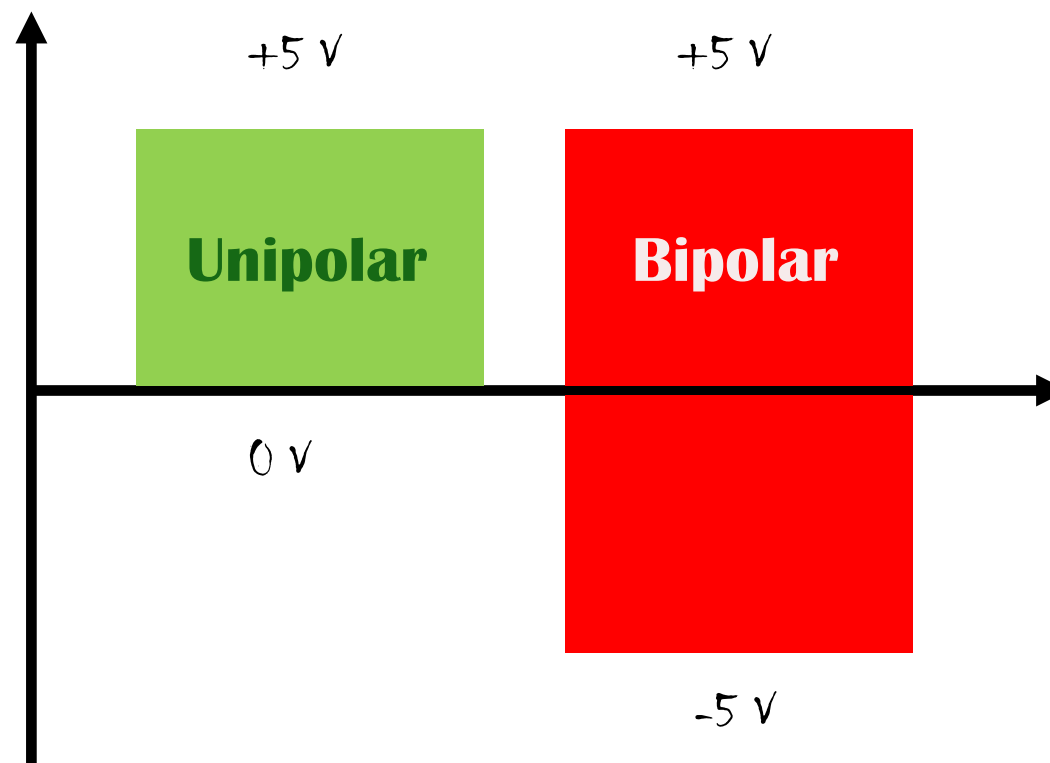
- **Analog-to-digital conversion** is the process of converting the output of the sample-and-hold circuit to a series of binary codes that represent the amplitude of the analog input at each of the sampling times.
- The sample-and-hold process keeps the magnitude of the analog input constant between sampling pulses, therefore analog-to-digital conversion can be done using a constant value.



Quantization of stair-step waveform into binary information

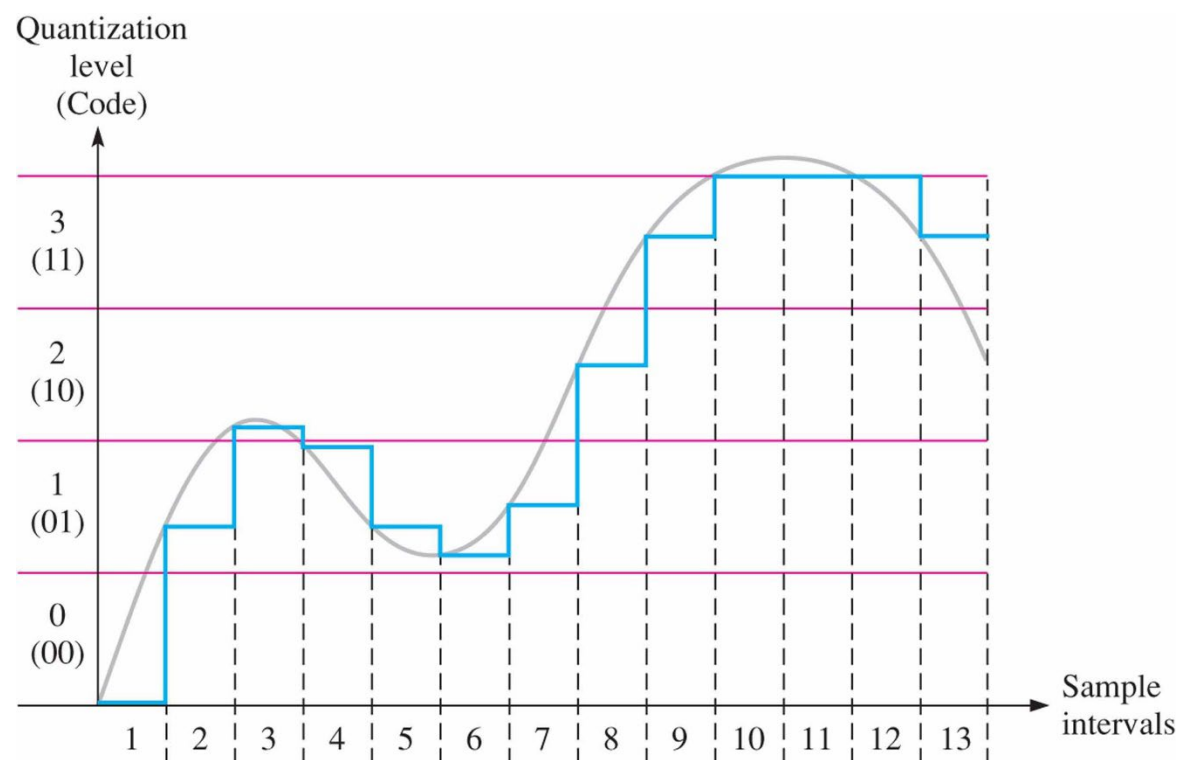
ADC Specifications: Range

- The input **range** of an ADC refers to the span of voltages that it can convert.
 - ✦ The end points of the range (called **rails**) are referred to as:
 - ✦ Lowest value ~ **-full-scale**.
 - ✦ Highest value ~ **+full-scale**.
- If the input voltage falls outside of the range, the ADC is said to be **overranged** and returns the value of the nearest end-point.

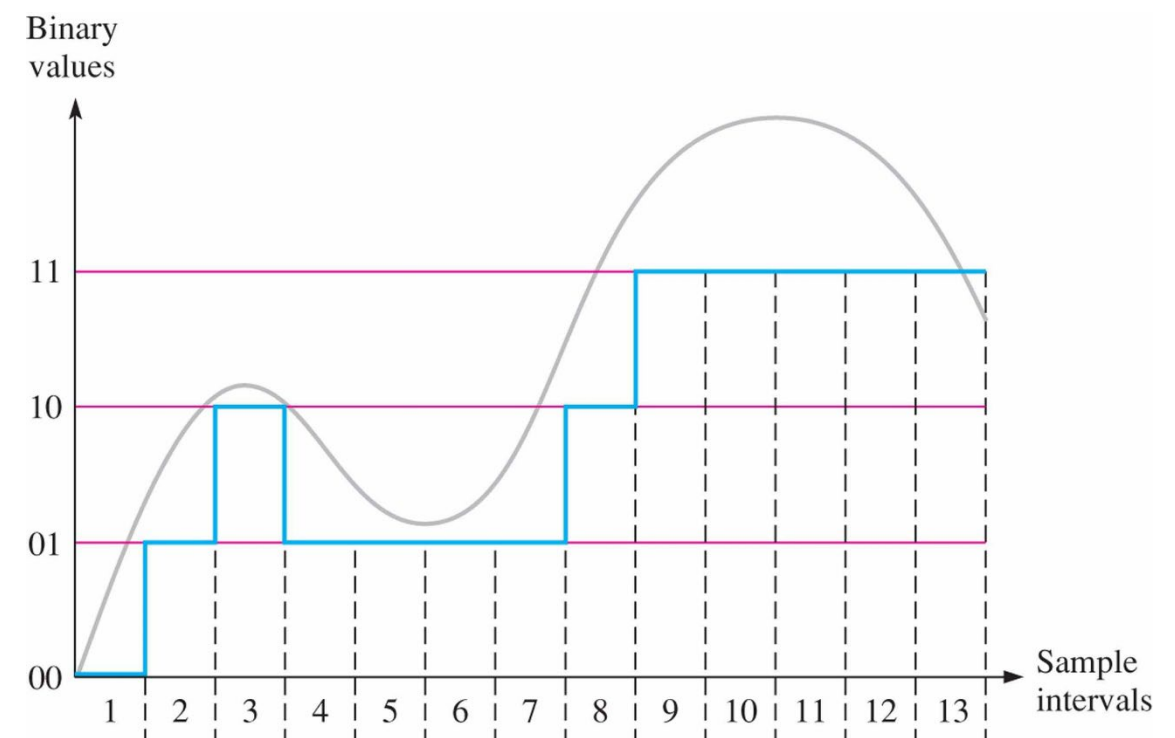


ADC Specifications: Resolution

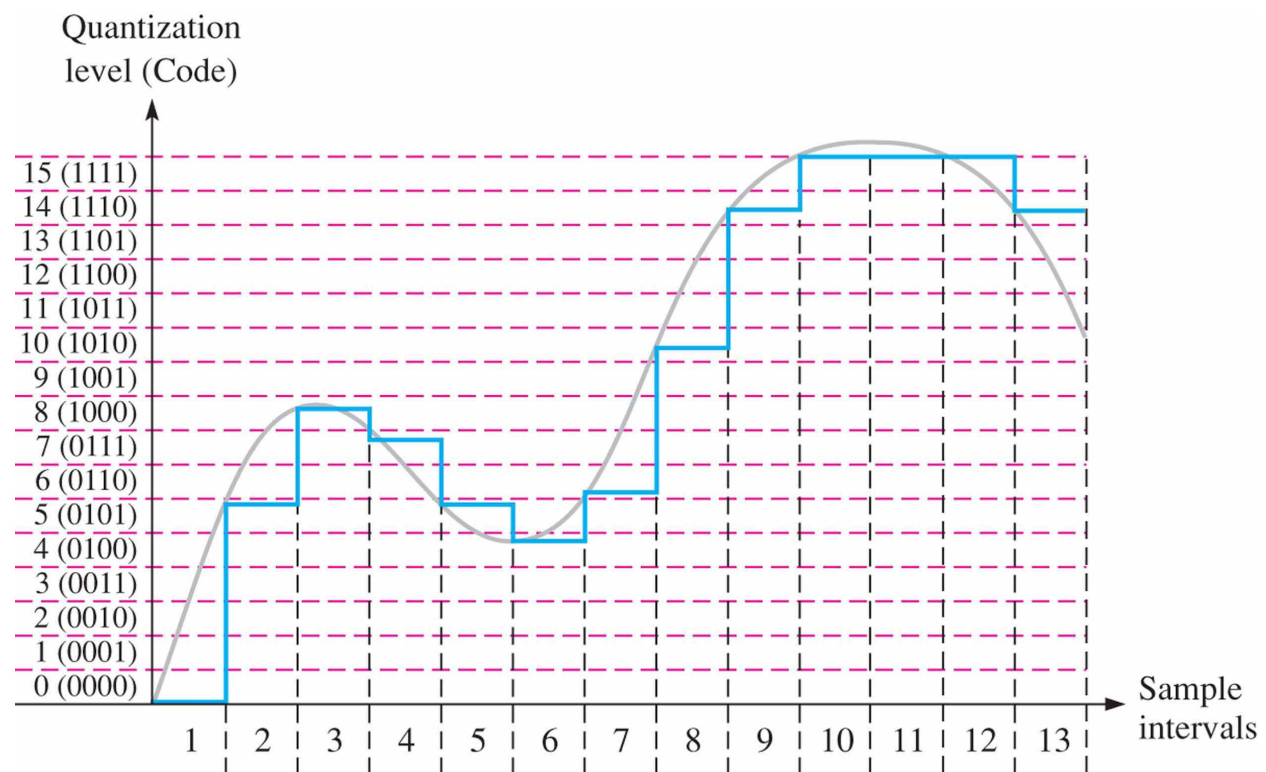
- The process of converting an analog value to a code is called **quantization**, during which the ADC converts each sampled value of the analog signal to a binary code.
- The more bits that are used to represent a sampled value, the more accurate is the representation. This is referred to as the **resolution** of the ADC.
- Using these quantized values, the original waveform can be reconstructed using a **digital-to-analog converter** (DAC).



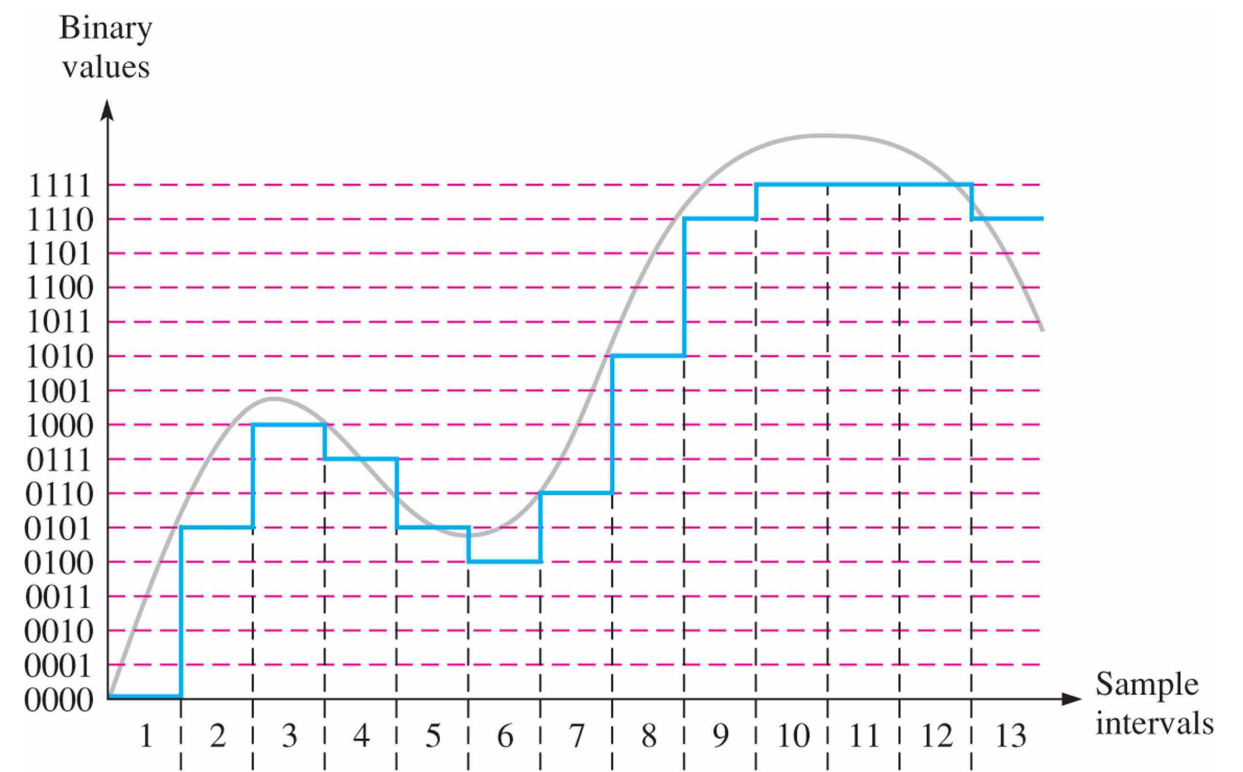
Original sampled waveform
with 2-bit resolution



Reconstructed waveform
with 2-bit resolution



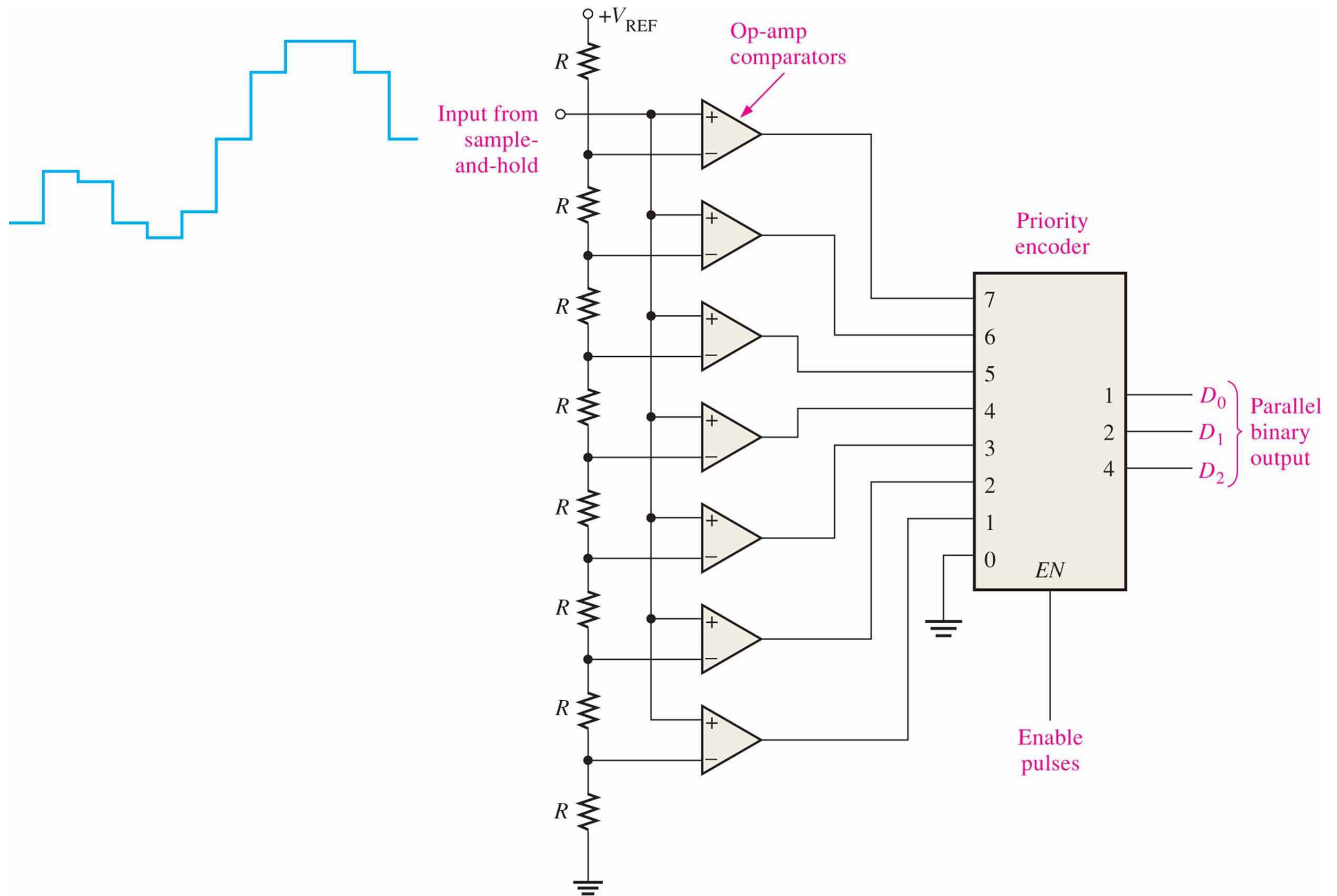
**Original sampled waveform
with 4-bit resolution**



**Reconstructed waveform
with 4-bit resolution**

Flash (Simultaneous) ADC

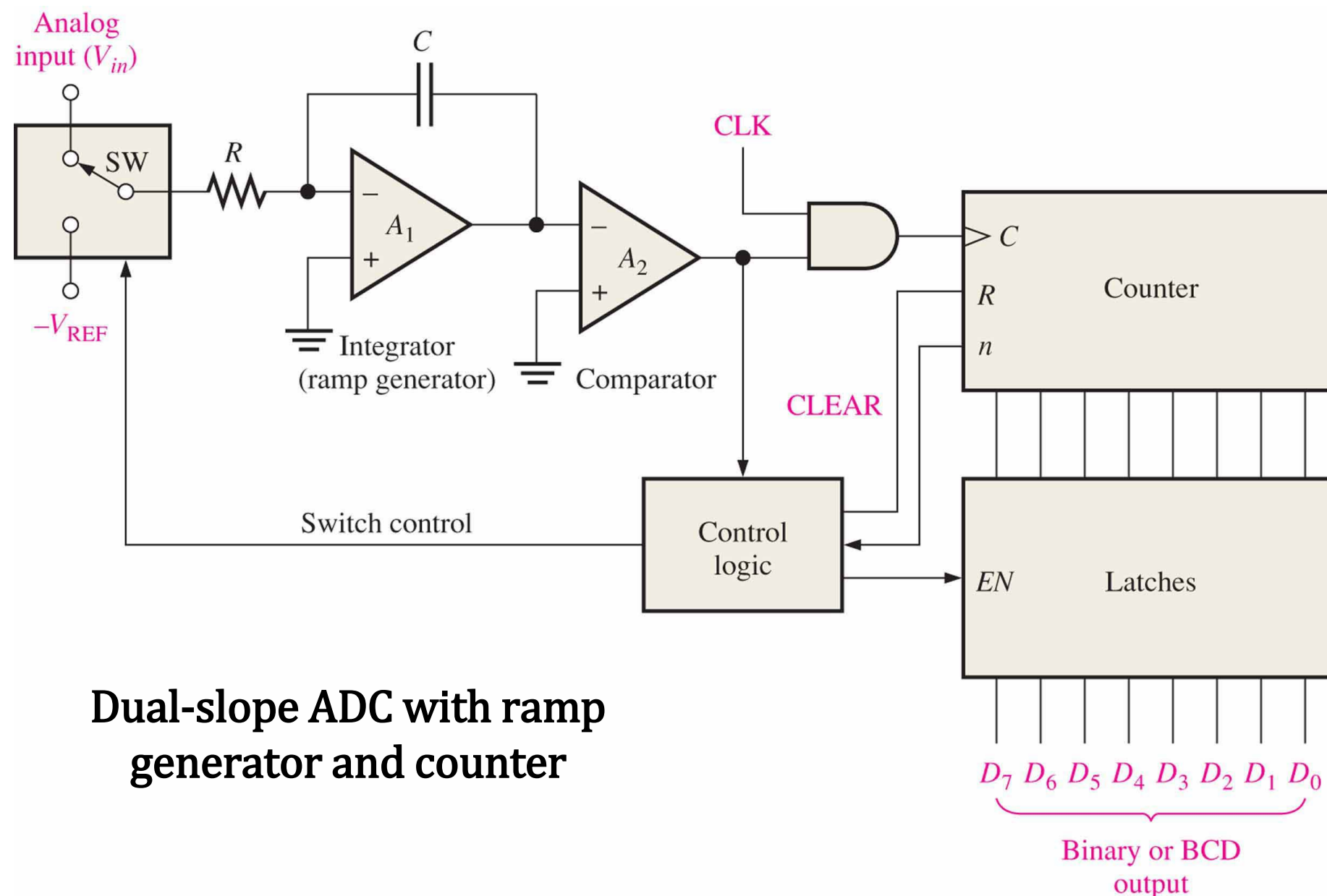
- The **flash method** utilizes comparators that compare reference voltages with the analog input voltage. When the input voltage exceeds the reference voltage for a given comparator, a HIGH is generated.
- A 3-bit converter requires seven comparators, a 4-bit converter requires fifteen comparators, etc.
- The number of bits used in an ADC is its **resolution**.
- The large number of comparators necessary for a reasonable-sized binary number is one of the disadvantages of the flash ADC.
- However, its main benefit is that it provides a fast conversion time because of a high throughput, measured in **samples per second**.
- The reference voltage for each comparator is set by the **resistive voltage-divider circuit**. The output comparator is connected to an input of the **priority encoder**.

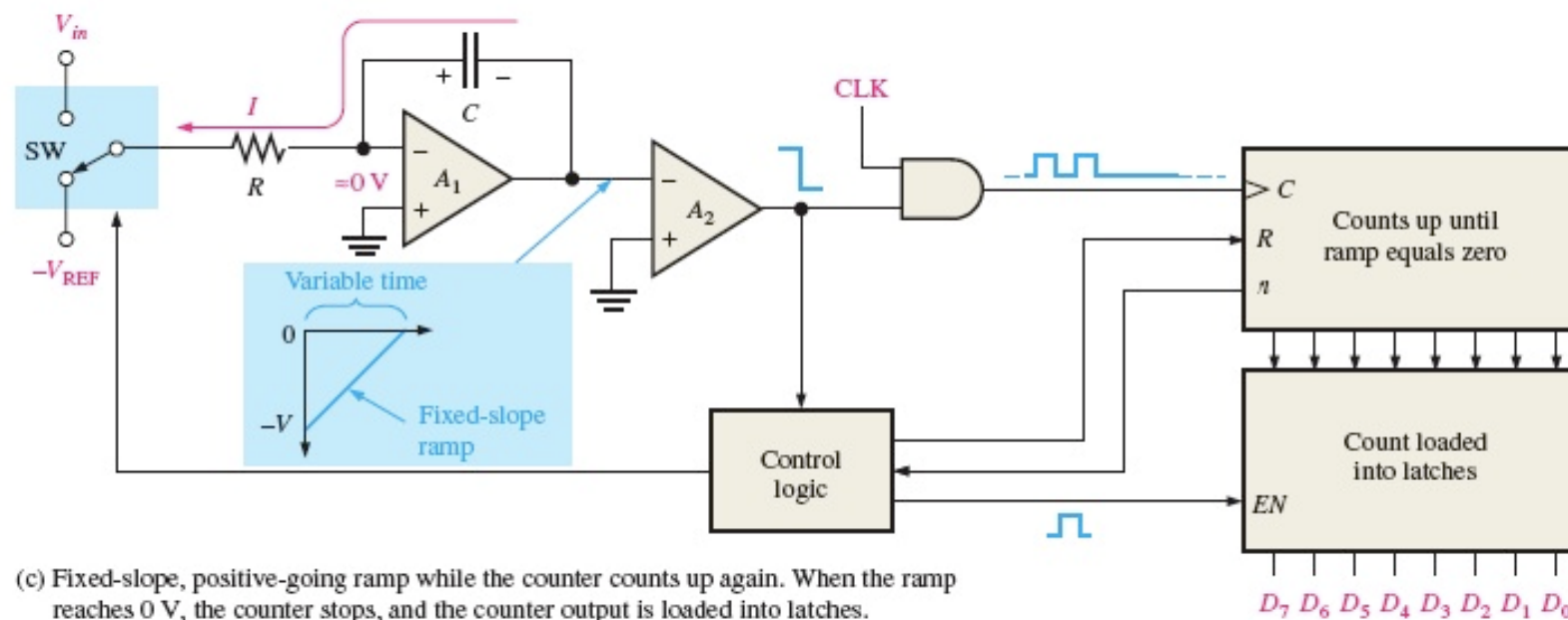
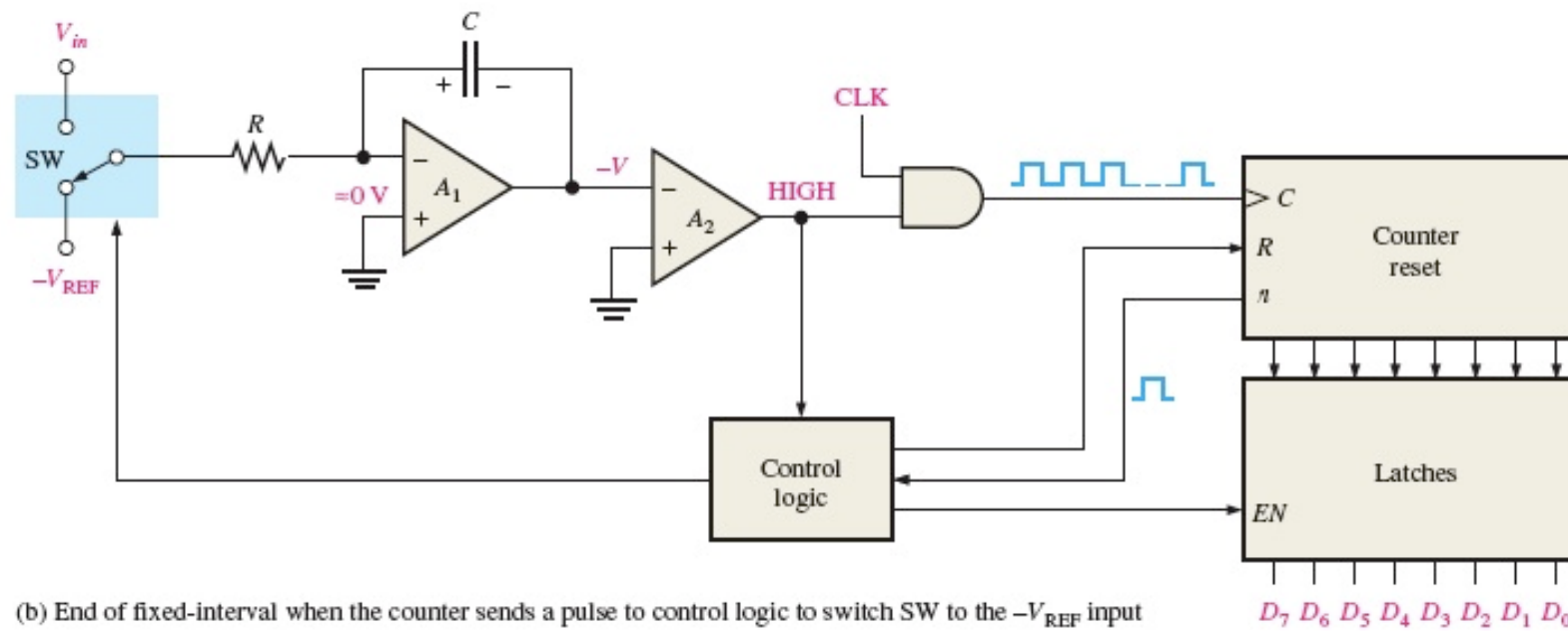
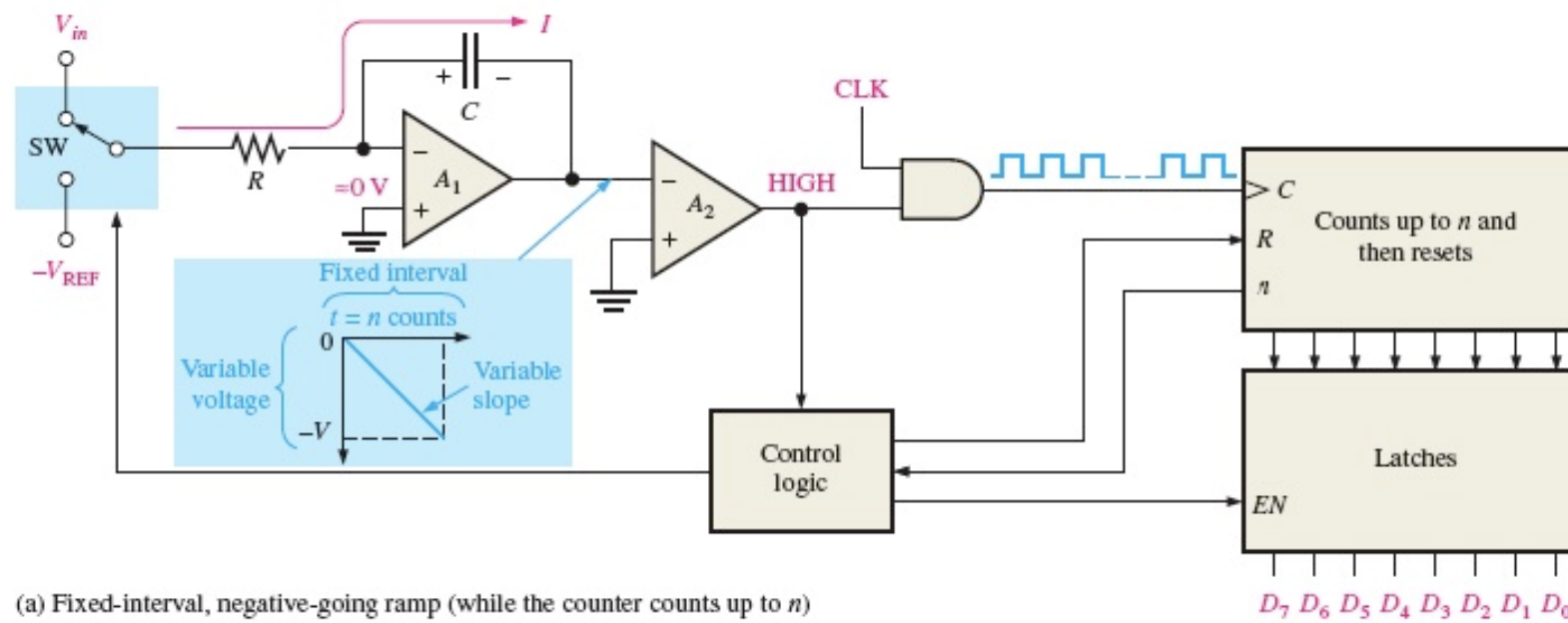


Flash or simultaneous ADC using multiple comparator op-amps

Dual-Slope ADC

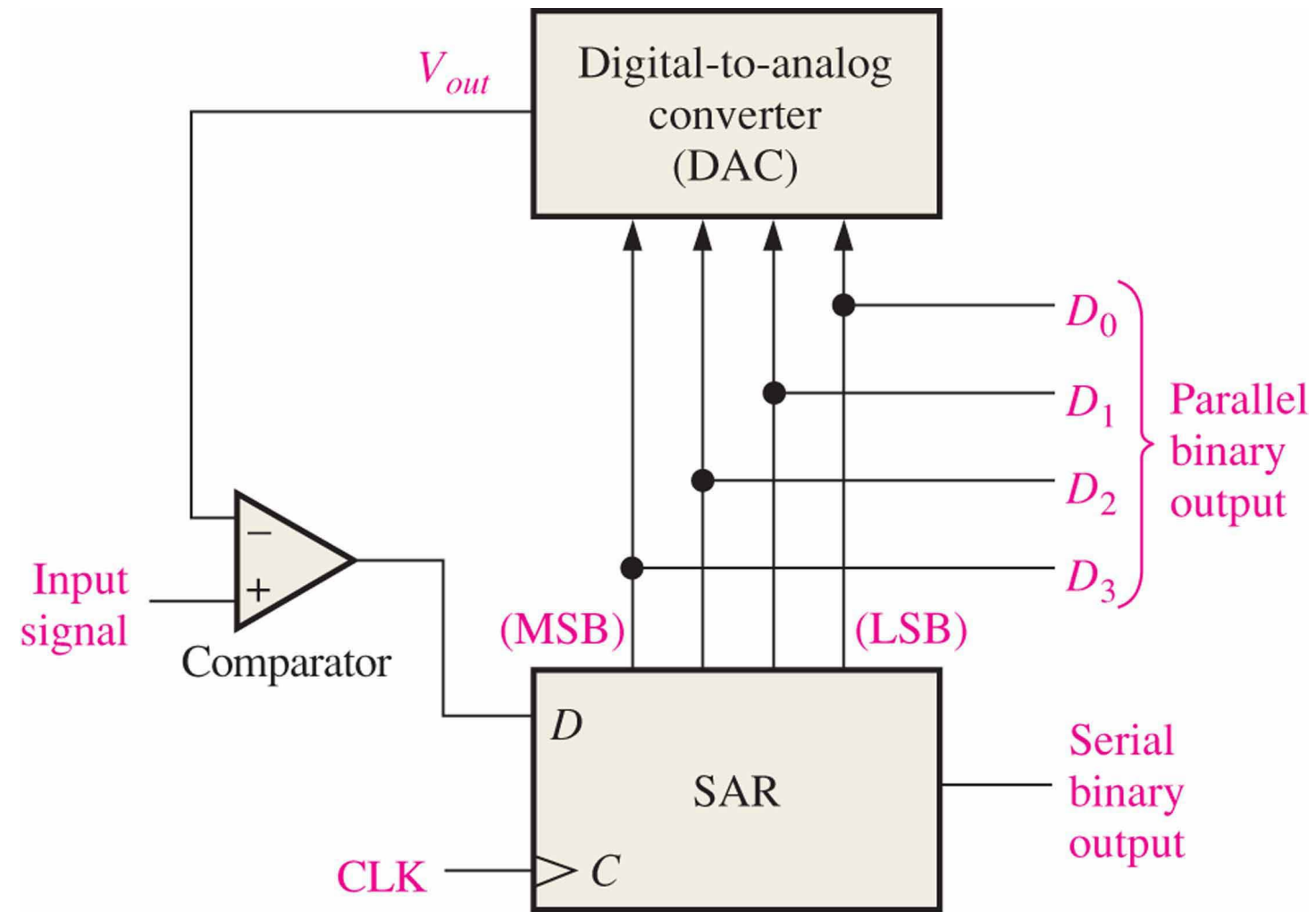
- A **dual-slope ADC** is common in digital voltmeters and other types of measurement instruments. A **ramp generator** (integrator) is used to produce the dual-slope characteristics.



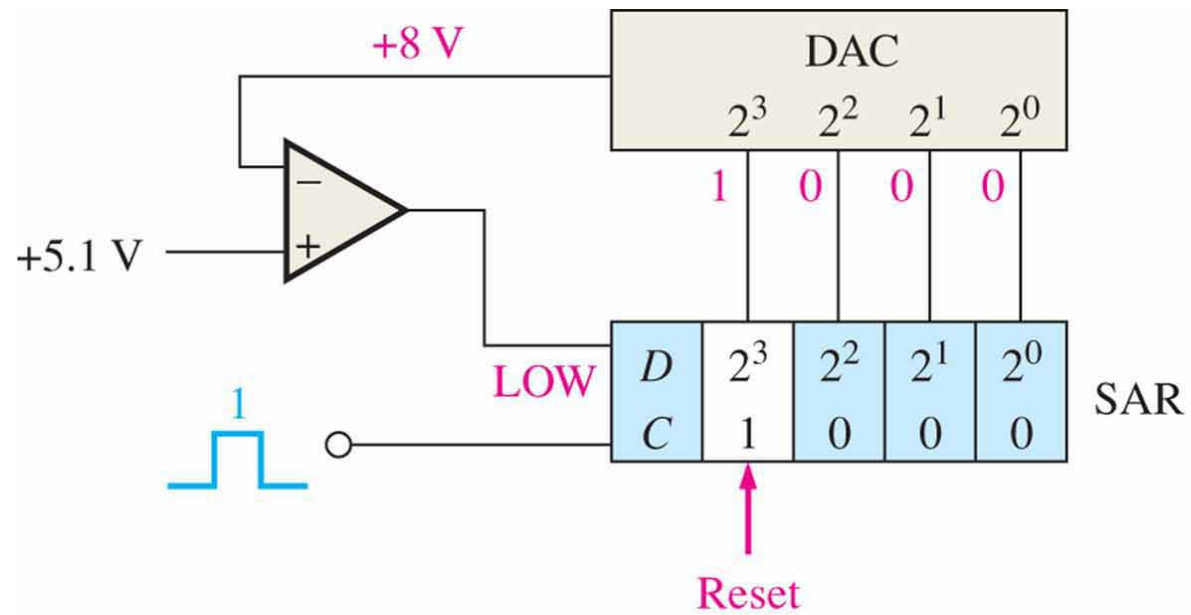


Successive-Approximation ADC

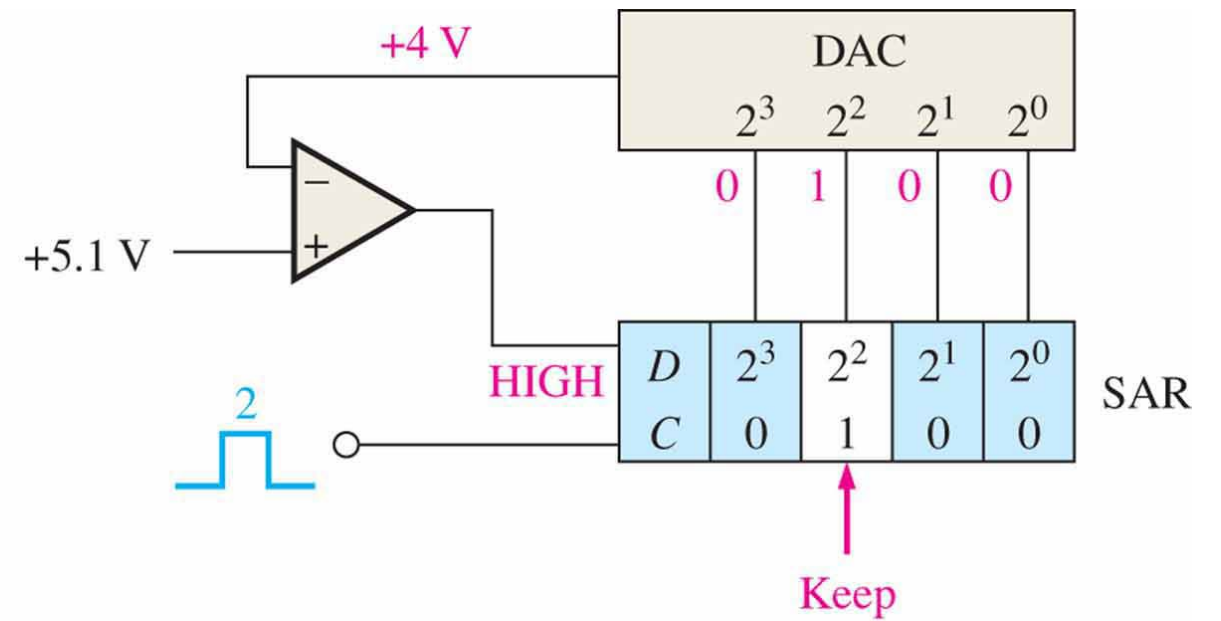
- One of the most widely used methods of ADC is **successive-approximation**, which has a much faster conversion time than the dual-slope conversion but is slower than the flash method.
- The successive-approximation ADC consists of a DAC, a **successive-approximation register** (SAR), and a comparator.
- The basic operation is as follows:
 - ✦ The input bits of the DAC are enabled one at a time, starting with the most-significant bit (MSB).
 - ✦ As each bit is enabled, the comparator produces an output that indicates whether the input signal voltage is greater or less than the output of the DAC.
 - ✦ If the DAC output is greater than the input signal, the comparator's output is LOW, causing the bit in the register to reset.
 - ✦ If the output is less than the input signal, the 1 bit is retained in the register.
 - ✦ This process is repeated until all the bits of the DAC has been tried.



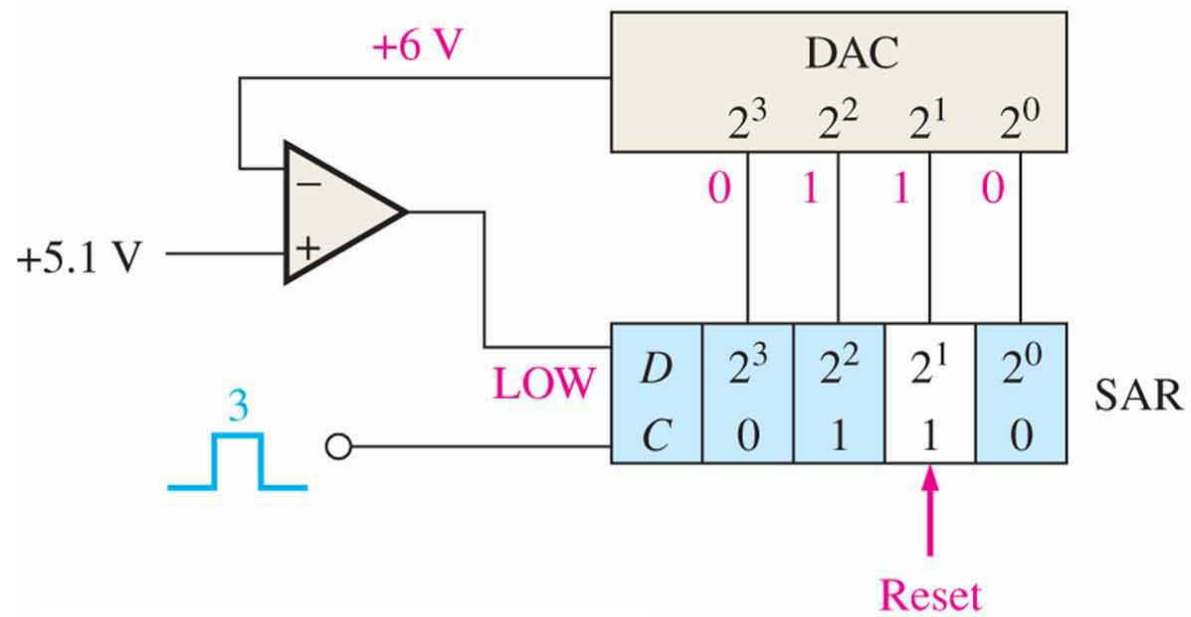
Successive-approximation ADC



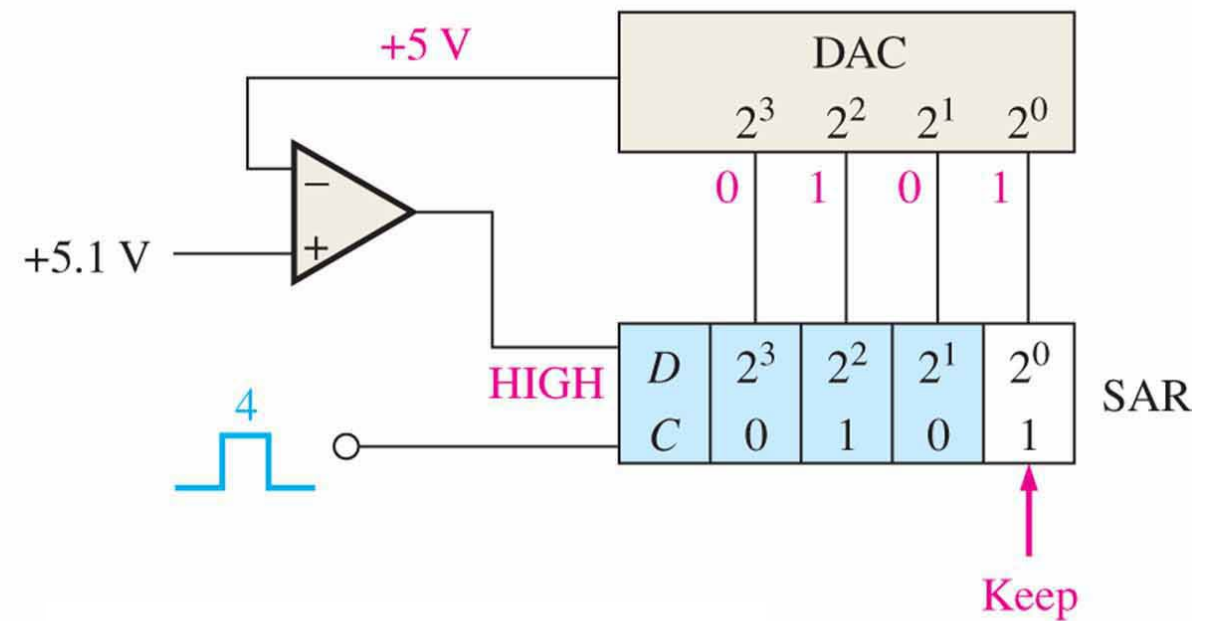
MSB comparison



2^2 -bit comparison



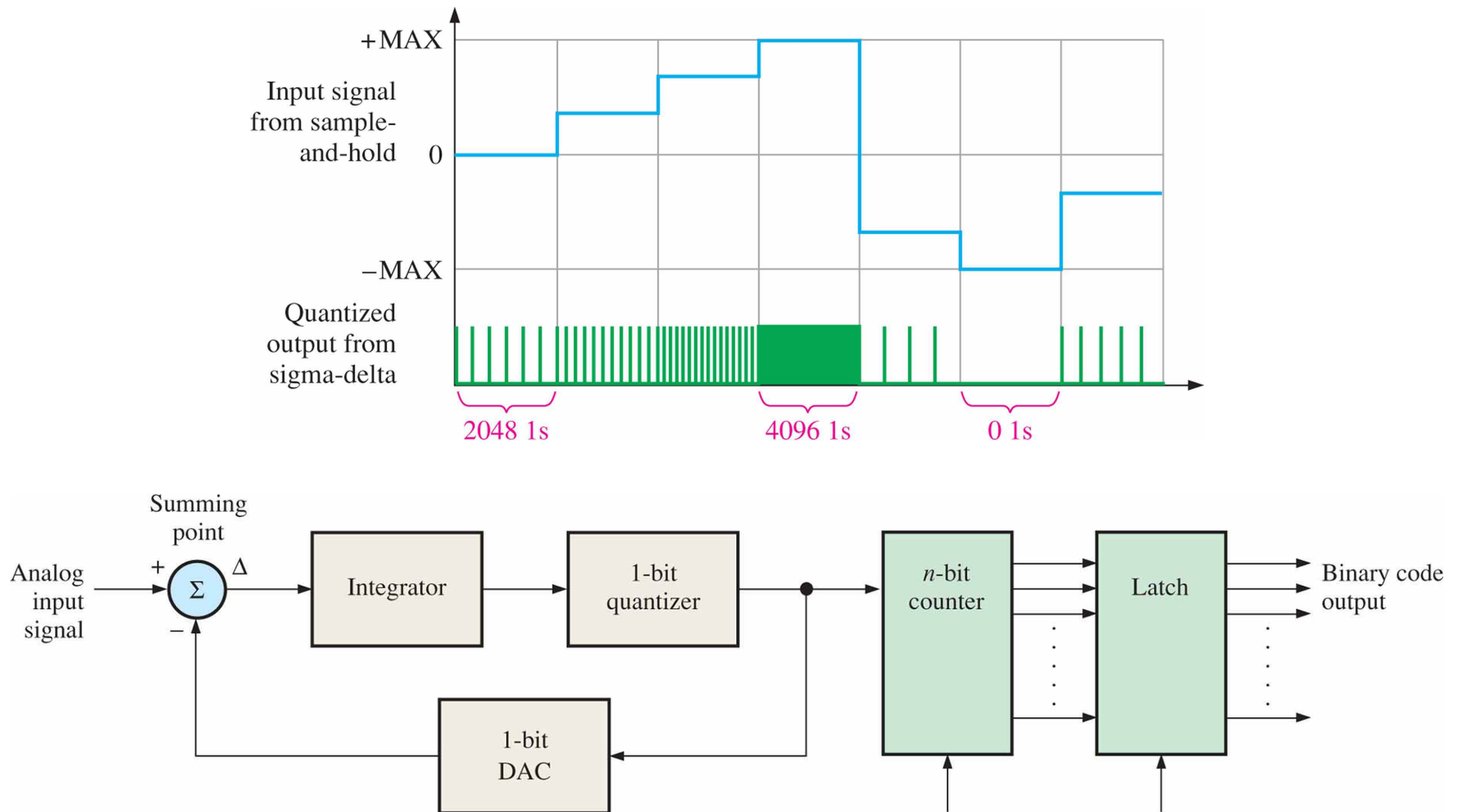
2^1 -bit comparison



LSB comparison

Sigma-Delta ADC

- **Sigma-delta** is another widely used method of ADC, especially in telecommunication systems.
- It is based on **delta modulation** where the difference between two successive samples (increase or decrease) is quantized. Delta modulation is a 1-bit quantization method.
- The output of the delta modulator is a single-bit data stream where the relative number of 1s and 0s indicates the level or amplitude of the input signal. The number of 1s over a given number of clock cycles establishes the signal amplitude during that interval.
 - ✦ A maximum number of 1s corresponds to the maximum (positive) input voltage.
 - ✦ A number of 1s equal to one-half the maximum corresponds to an input voltage of zero.
 - ✦ No 1s (all 0s) corresponds to the minimum (negative) input voltage.
- In other words, the number of 1s is proportional to the analog input signal level.

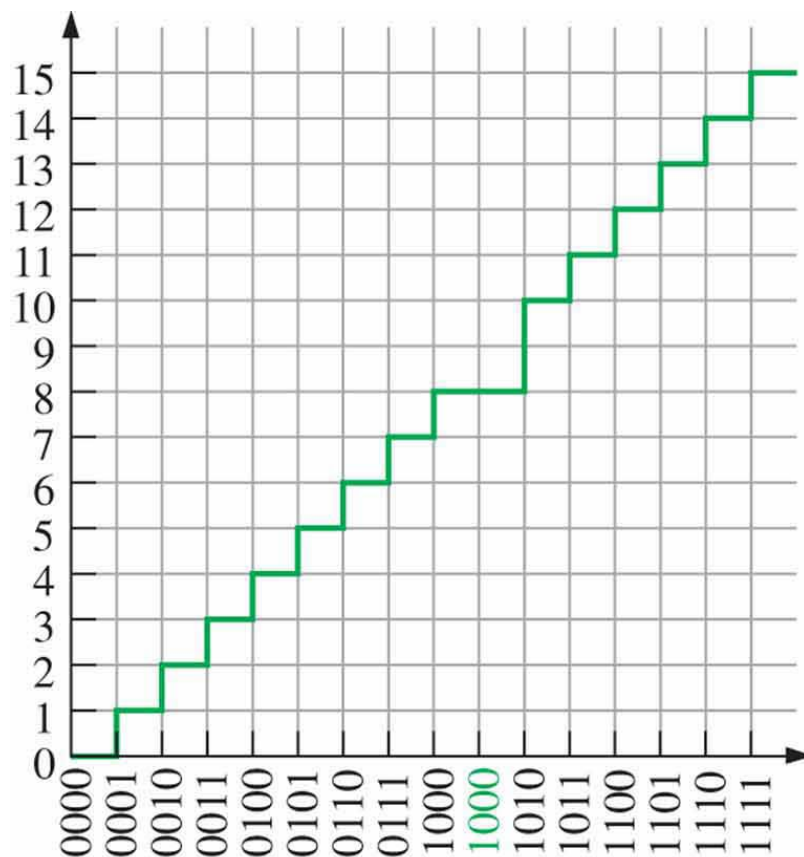


Sigma-delta ADC with 1-bit quantizer and counter

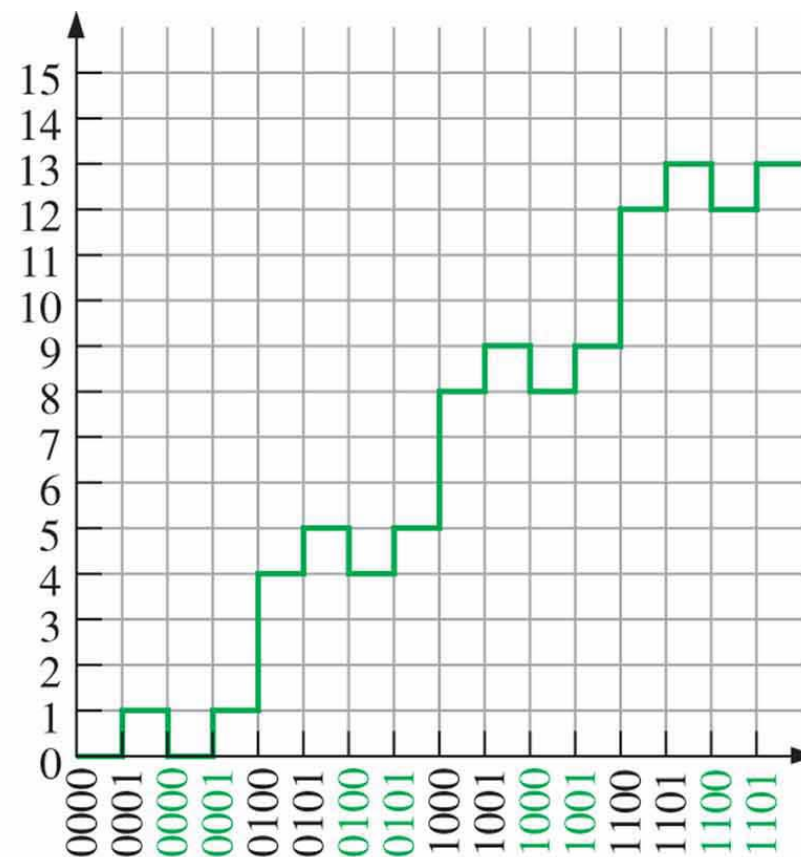
- The above block diagram illustrates a sigma-delta ADC. The 1-bit quantizer essentially functions as a comparator followed by a latch. The single-bit data stream is then passed to a counter and latch to produce the binary code output.

ADC Errors

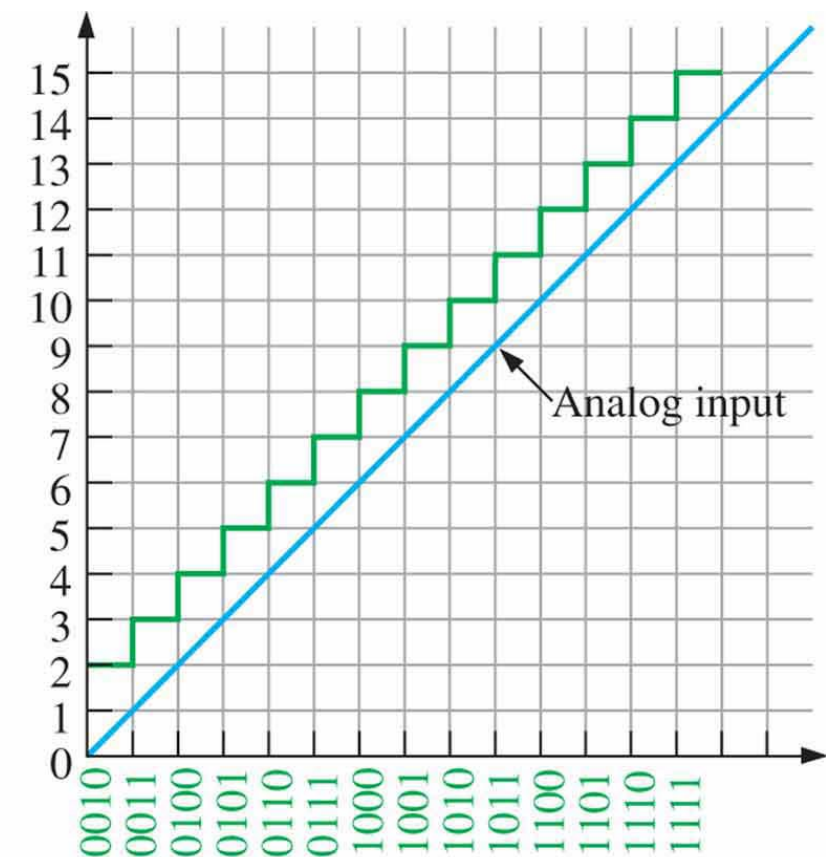
- The main types of error that commonly occur during ADC are:
 - ♦ **Missing code** ~ in flash ADC, this may be caused by a failure of one of the op-amp comparators.
 - ♦ **Incorrect codes** ~ may occur when some bits are stuck in a particular state.
 - ♦ **Offset** ~ the ADC interprets the analog input voltage as greater or less than its actual value.



Missing code



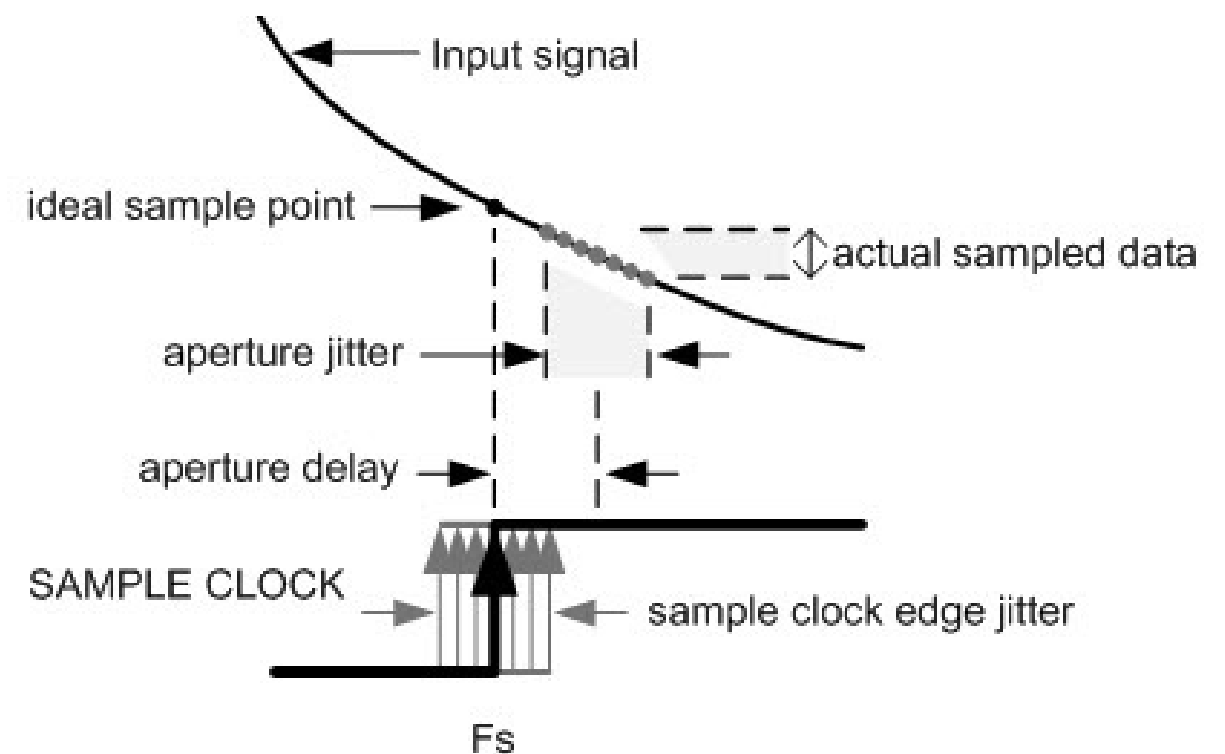
Incorrect codes



Offsets

Aperture Delay and Jitter

- All ADCs require a **clock signal** to know when to start conversion.
- There is always a small amount of delay between when the signal is held and when the ADC begins to operate. This is called the **aperture delay**. The effects of aperture delay is negated by the presence of other circuitry in front of the ADC.
- **Aperture jitter** refers to the difference in the amount of time between samples that can lead to interference at frequencies very close to the signal of interest. This can be caused by:
 - ✦ Clock source.
 - ✦ Digital clock circuitry
 - ✦ Sample-and-hold circuit.



Aperture delay and jitter

Binary-Weighted Input DAC

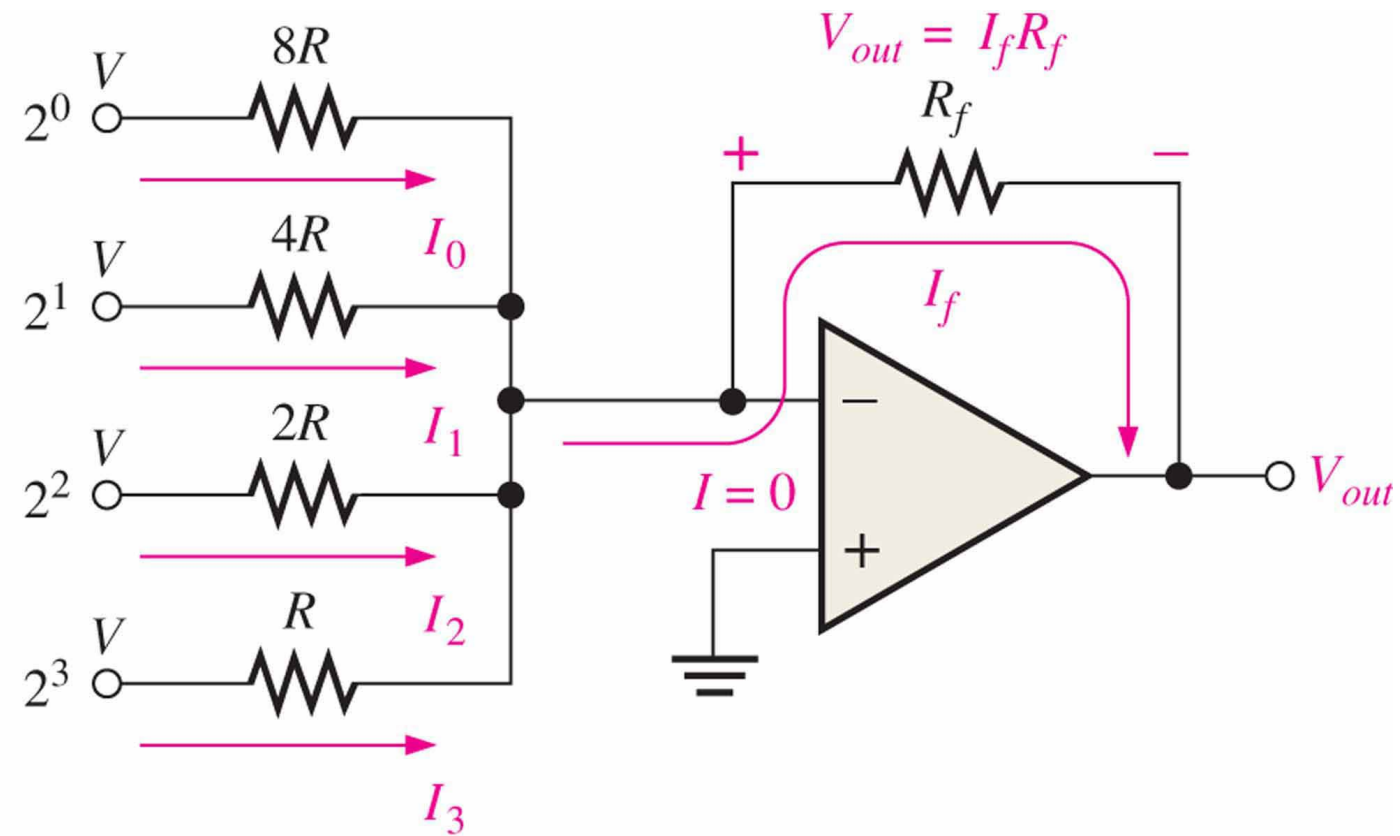
- The **binary-weighted input DAC** uses a resistor network with resistance values that represent the binary weights of the input bits of the digital code.
- Each of the input resistors will either have a current or have no current, depending on the input voltage level.
 - ✦ If the input voltage is zero, the current is also zero.
 - ✦ If the input voltage is HIGH, the amount of current depends on the input resistor value and is different for each input resistor.
- Since there is practically no current into the op-amp inverting input, all of the input currents sum together and go through R_f . Since the inverting input is at 0 V, the drop across R_f is equal to the output voltage, so $V_{\text{out}} = I_f R_f$.
- The values of the input resistors are chosen to be inversely proportional to the binary weights of the corresponding input bits.
- The disadvantages of this type of DAC are the number of different resistor values and the fact that the voltage levels must be exactly the same for all inputs.

$$I_0 = \frac{V}{8R}$$

$$I_1 = \frac{V}{4R}$$

$$I_2 = \frac{V}{2R}$$

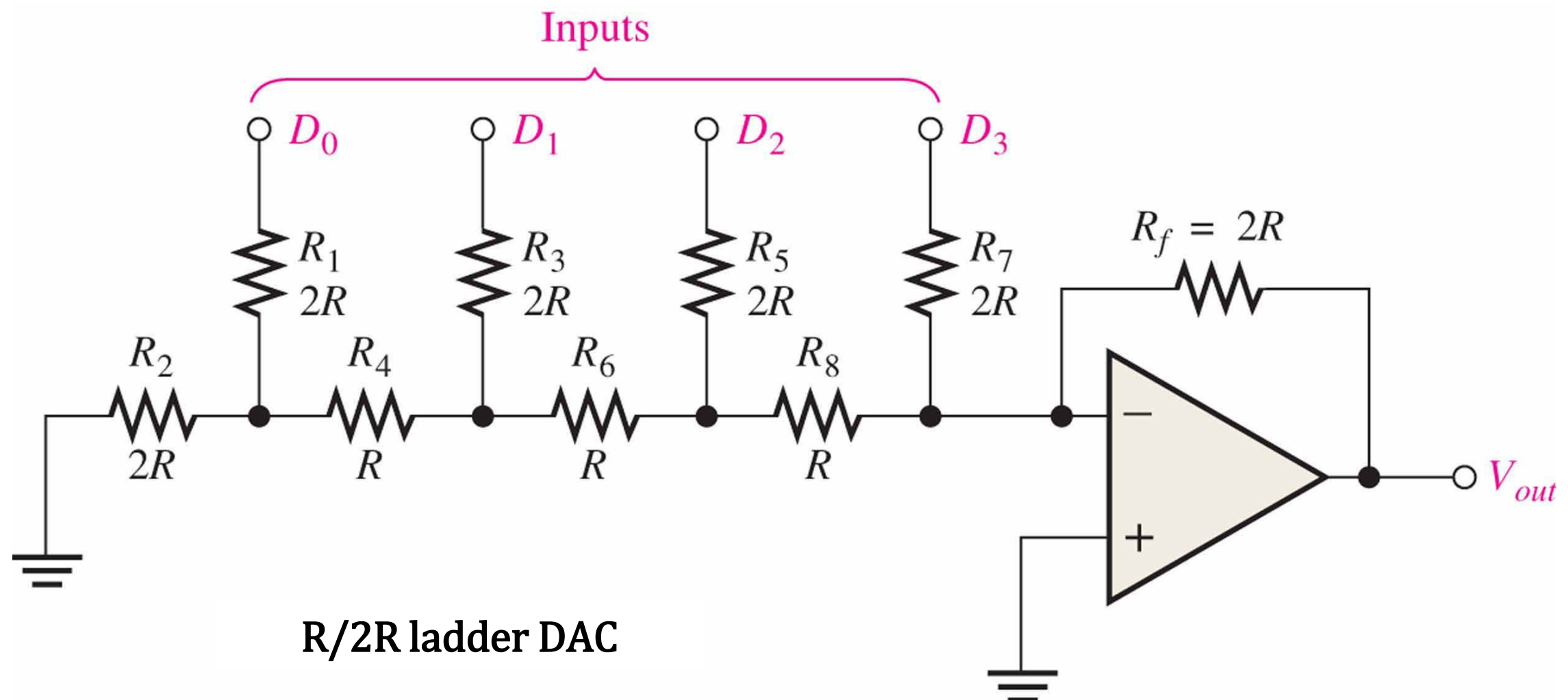
$$I_3 = \frac{V}{R}$$



Binary-weighted DAC

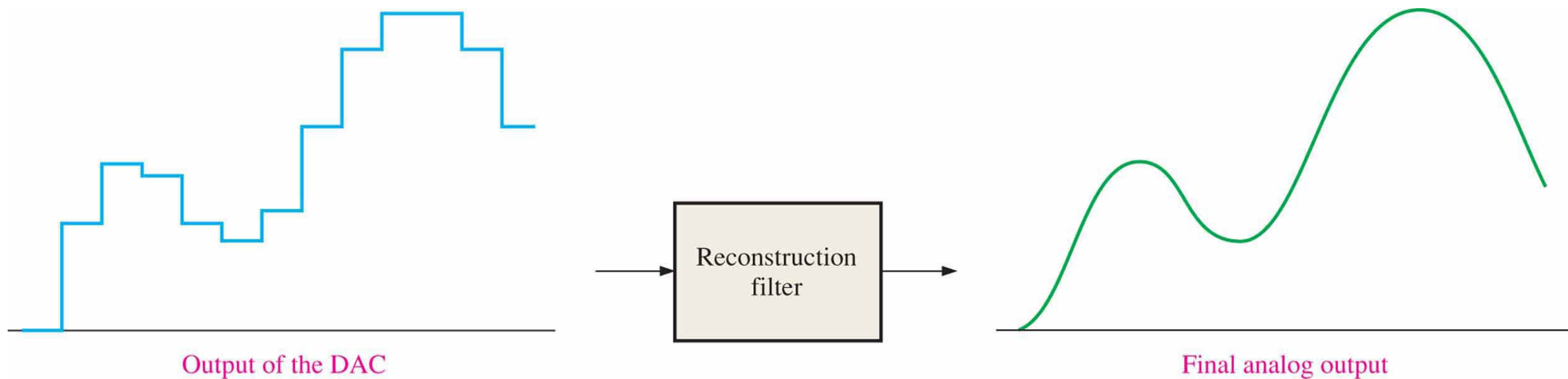
R/2R ladder DAC

- The **R/2R ladder** is another method for DAC. It overcomes one of the problem of the binary-weighted input DAC in that it requires only two resistor values.
- Notice that each successively lower-weighted input produces an output voltage that is halved, so the output voltage is proportional to the binary weight of the input bits.



Reconstruction filter

- The output of the DAC is a stair-step approximation of the original analog signal after it has been processed by the DSP.
- The purpose of the **reconstruction filter** or **post-filter** is to smooth out the DAC output by eliminating the higher frequency content that results from the fast transitions of the stair-steps.

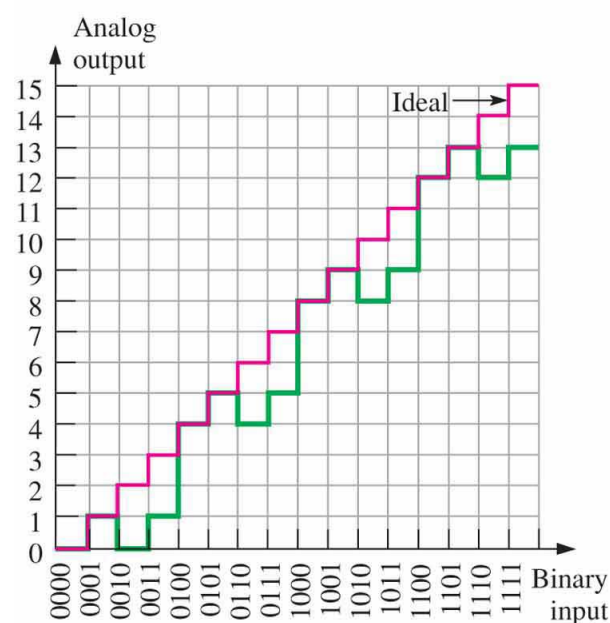


Reconstruction filter smooths out the stair-step waveform

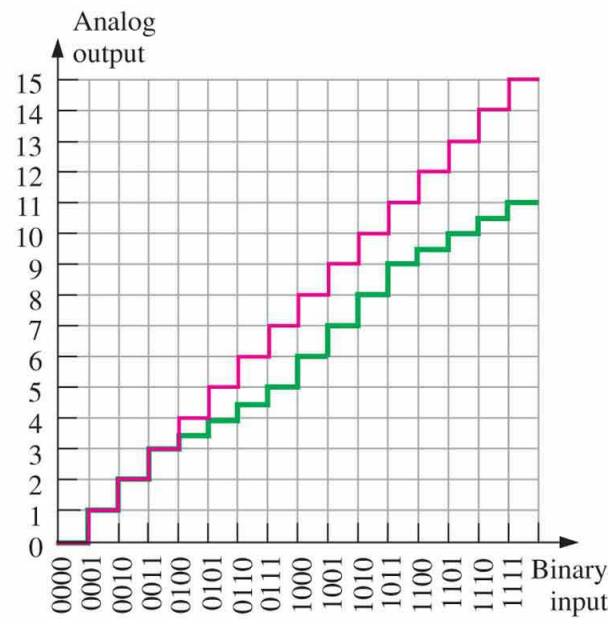
DAC Errors

■ The main types of error that commonly occur during DAC are:

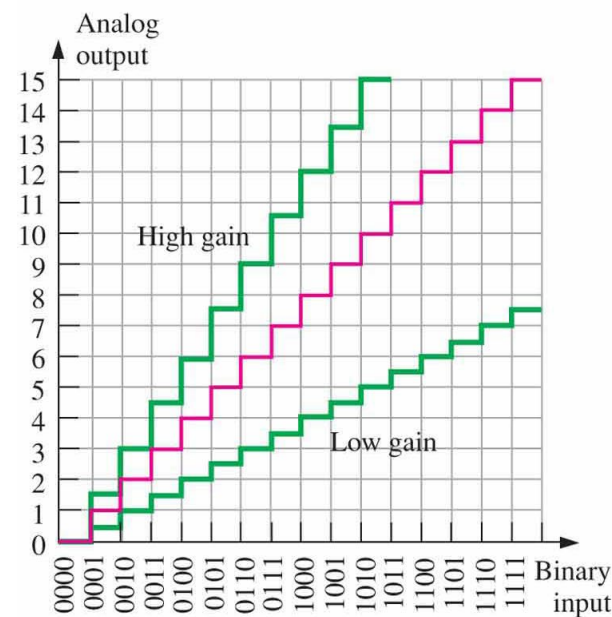
- ♦ **Non-monotonicity** ~ a form of nonlinearity that occurs because a bit input line is stuck.
- ♦ **Differential nonlinearity** ~ caused by insufficient weight at certain bits due to a faulty input resistor.
- ♦ **Low or high gain** ~ caused by a faulty feedback resistor in the op-amp circuit.
- ♦ **Offset error** ~ may be caused by a faulty op-amp.



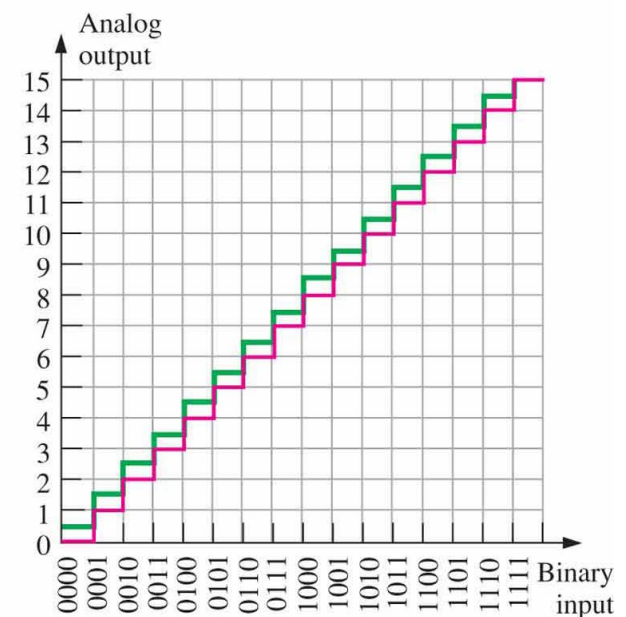
Non-monotonic
output



Differential
nonlinearity



High and low
gains



Offset error